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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/519,867	MA, FAN YUNG	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1,2 and 4-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of Changes

1. The objection to the drawings has been overcome by the replacement drawing sheets filed 21 February 2006.
2. The rejection of claims 4-7 under 35 U.S.C. § 112 second paragraph with have been overcome by Applicant's amendment and remarks

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by Winebarger (USPN 4,260,907).

With respect to claim 1 Winebarger discloses in Fig. 2, a detection circuit for monitoring a supply voltages the circuit comprising:

"a comparator (46) for generating a shortfall signal (it can be seen that 46 outputs a short fall signal, while V+ is to low for operation) indicative of a shortfall of the supply voltage (V+ at node 12 is supplied to node 42 of 46 through R1) in relation to a reference voltage (voltage at the – terminal of 46 at node 44), and an integrator for time-integrating the shortfall signal to form an integrated signal (R4 and C2 form an

integrator, R4 and C2 integrate the short fall signal (output of 58)), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor (it can be seen that the output of the integrator is supplied as a power-on reset signal at the output of inverter 60. "for resetting a microprocessor" is merely function language that is provided by the circuit in Fig. 2 of Winebarger, it can be seen that 62 is a POR signal. It would be apparent to one of ordinary skill in the art that POR signals are used to reset microprocessors. Thus, Winbarger's circuit is capable of performing the intended use of resetting a microprocessor with its POR signal.)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Winebarger (4,260,907). Winebarger teaches, in Fig 2 the circuit recited in claim 4. Winebarger does not explicitly teach the use of the circuit in Fig. 3 with a microprocessor. However, Winebarger discloses (in Col. 1 lines 6-17) that the invention "lies in the field of electronic equipment", and more specifically electronic equipment in which problems arise when "the power supply to the equipment fails". Winebarger also discloses that this detection circuit can be used in electronic equipment where "there

are one or many, flip flops, adders, registers, counters, etc." It would be obvious for one skilled in the art at the time of the invention to include microprocessors in this "electronic equipment" category, because microprocessors are commonly composed of the above list of "electronic equipment". Additionally, a microprocessor would be included in the above mentioned "electronic equipment". Thus, it is obvious that Winebarger teaches the use of the above reset circuit to reset microprocessors.

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to reset a microprocessor with Winebargers above recited reset circuit for the purpose of having a simply a simply constructed power-on reset circuit that resets when the supply voltage drops below a certain level (See Col. 2 lines 5-15). One skilled in the art would have been motivated to combine the circuit of Winebarger with a microprocessor with a reasonable expectation of success.

With respect to claim 4, Winebarger as modified above discloses in Fig. 2, A circuit comprising:

"a microprocessor circuit; (the electronic component receiving the POR signal as modified above (not shown in Fig. 2) see Col. 1 lines 29-31))

a comparator (46) for generating a shortfall signal indicative of a shortfall of the supply voltage (V+ at node 12 is supplied to node 42 of 46 through R1) in relation to a reference voltage (voltage at the – terminal of 46 at node 44), and an integrator for time-integrating the shortfall signal to form an integrated signal (R4 and C2 form an integrator), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor circuit (it can be seen that the output of the integrator is

supplied as a power-on reset signal at the output of inverter 60, which is input to the microprocessor circuit as modified above), and

reset means arranged to receive the reset signal output by the UVD circuit and according to its value to initiate a reset of the microprocessor circuit." (Since it is obvious to use the reset signal of Winebarger with a microprocessor, it is inherent that the microprocessor has a means to receive the reset signal, which is being used to reset the microprocessor circuit as modified above).

With respect to claim 5, Winebarger as modified above discloses in Fig. 2, a method including:

"generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage (46 outputs at 58 a signal that detects if the signal ant 42 of 46 is lower than the signal at 44 of 46), time-integrating the shortfall signal to form an integrated signal (R4 and C2 act as integrator, which integrates the output of 58), and generating a reset signal using the shortfall signal, wherein the reset signal is for resetting a microprocessor (as explained above it would be obvious to use the circuit of Fig. 2 to reset a microprocessor)."

With respect to claim 6, Winebarger as modified above discloses in Fig. 2, the method of claim 5 and further comprising resetting the microprocessor with the reset signal. (as disclosed above it is obvious to use the reset signal to reset the microprocessor.)"

Claims 1-2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Yoshimura (5,629,642) in view of Woods (USPN 6,259,285). Yoshimura teaches, in Fig. 1 a comparator detects a shortfall in a supply by receiving a supply voltage and a reference voltage. The output of the comparator is input to a discriminator circuit, and a delay circuit, which is used to prevent a reset when the power supply voltage is instantaneously decreased. It is used to delay the comparators signal by a prescribed amount of time. (See Col. 1 lines 51-58). This delay circuit also outputs a signal to the discriminator. The discriminator then outputs a reset signal based on the inputs of the delay and comparator circuits. Yoshimura does not teach an integrator circuit receiving the output of the comparator. Woods teaches, in Fig. 1 a delay circuit that integrates signals input to it. Woods' delay circuit as disclosed is used in a reset circuit that detects power loss. Additionally, Woods' delay circuit is used to "filter out rapid perturbations in the power supply voltage" (see Col. 2 lines 41-43).

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the specific delay circuit 130 of Woods in place of the generic delay circuit 7 of Yoshimura for the purpose of having a simply constructed delay circuit that is used to delay the voltage of comparator 4, to prevent an erroneous output of the RESET signal. One skilled in the art would have been motivated to combine Yoshimura and Woods with a reasonable expectation of success.

With respect to claim 1, the above combination of Yoshimura and Woods, discloses, a detection circuit for monitoring a supply voltages the circuit comprising:

"a comparator (4 of Fig. 1 of Yoshimura) for generating a shortfall signal indicative of a shortfall of the supply voltage (VCC is supplied to 4 through 2) in relation

to a reference voltage (5 supplies a reference voltage to 4, which is used with to Vcc to detect a shortfall in the supply voltage VCC.), and an integrator for time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 now includes the resistor and capacitor of 130 of Fig. 1 of Woods. This resistor and capacitor arrangement integrates and delays the signal of comparator 4 being input to circuit 7), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor (the integrator circuit 7 is input to discriminator circuit 10, which uses both signals form 7 and 4 to output a reset signal, the resetting of the microprocessor is deemed to be intended use, and the disclosed circuit provides the possibility of being used to reset a microprocessor.)."

With respect to claim 2, the above combination of Yoshimura and Woods discloses, a circuit according to claim 1 further including "a discriminator circuit for receiving the integrated signal (10 is a discriminator that receives the integrated signal c) and at least one further output of the comparator (it can be seen that 4 also additionally outputs a signal to circuit 10 at the node between 6 and 7), and generating a reset signal using the integrated signal and the at least one further output (10 uses both signals of the comparator and the integrated signal to output the reset signal e)."

With respect to claim 4, the above combination of Yoshimura and Woods discloses, "a microprocessor circuit (circuit being reset by not(RESET) signal, see Col. 2 lines 65 not(RESET) "signal for inactivating the memory or a control IC." Clearly a microprocessor is a control IC, in that it controls information input to it and is an integrated circuit)

a comparator (4 of Fig. 1 of Yoshimura) for generating a shortfall signal indicative of a shortfall of the supply voltage (VCC is supplied to 4 through 2) in relation to a reference voltage (5 supplies a reference voltage to 4, which is used with to Vcc to detect a shortfall in the supply voltage VCC.), and an integrator for time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 now includes the resistor and capacitor of 130 of Fig. 1 of Woods. This resistor and capacitor arrangement integrates and delays the signal of comparator 4 being input to circuit 7), wherein the output of the integrator is used to generate a reset signal for resetting a microprocessor circuit (the integrator circuit 7 is input to discriminator circuit 10, which uses both signals form 7 and 4 to output a reset signal, the resetting of the microprocessor is deemed to be intended use, and the disclosed circuit provides the possibility of being used to reset a microprocessor.), and

reset means arranged to receive the reset signal outputted by the UVD circuit according to it value to initiate a reset of the microprocessor (Yoshimura discloses in Col. 1 lines 7-9, that the circuit can be used to monitor power supply for a voltage drop in an apparatus that needs back-up of data. It is obvious to one skilled in the art use Yoshimura's circuit to reset and detect a voltage drop in the supply voltage of a microprocessor, since they are known to be used to "back-up data". Thus it would be inherent that the microprocessor had a means to receive the reset signal, that is provided to it by Yoshimura's circuit.)."

With respect to claim 5, the above combination of Yoshimura and Woods discloses, "a method of monitoring a supply voltage including:

generating a shortfall signal indicative of a shortfall of the supply voltage in relation to a reference voltage (a shortfall signal is generated by 4 detecting when the Vcc drops below reference voltage 5); time-integrating the shortfall signal to form an integrated signal (the modified delay circuit 7 time integrates the output of 4 by low pass filtering the output of 4); and generating a reset signal using the shortfall signal, wherein the reset signal is for resetting a microprocessor (as explained above the it would be obvious to use reset signal e, which is generated form the output signals of 4 and 7, to reset a microprocessor)."

With respect to claim 6, the above combination of Yoshimura and Woods discloses, the method of claim 5 and further comprising resetting the microprocessor with the reset signal (as stated above it would be obvious to use the reset signal e to reset a microprocessor)."

With respect to claim 7, the above combination with Yoshimura and Woods discloses, the circuit according to claim 4, wherein the UVD circuit further includes a discriminator circuit (10) for receiving the integrated signal (output of 7 c) and at least one further output of the comparator (output of 4 between the out of 6 and then input of 7), and generating a reset signal using the integrated signal and the at least one output (it can be seen that the RESET signal e is generated by 10, by receiving the signals output by 4 and 7).

Response to Arguments

With respect to claim 1 rejected under 35 USC 102 (b) as being anticipated by

Winebarger (USPN 4,260,907), examiner finds Applicant's arguments unpersuasive. Clearly the recitation of "for resetting a microprocessor" is intended use. Winebarger is capable of resetting a microprocessor (Winebarger discloses, in Col. 1 lines 6-17, that the invention "lies in the field of electronic equipment", and more specifically electronic equipment in which problems arise when "the power supply to the equipment fails", and "If the voltage drops below [a] value then it is imperative to reset the equipment" (see Col. 1 lines 29-31). Clearly a microprocessors are "electronic equipment", thus Winebarger is capable of resetting a microprocessor. Therefore Winebarger anticipates this functional language.

Applicant asserts that Winebarger does not disclose "a comparator for generating a shortfall signal indicative of a shortfall supply voltage in relation to a reference voltage", and "the outputs of the integrator is used to generate a reset signal for resetting a microprocessor". However, as indicated previously and in the above rejection, Winebarger does disclose these elements. Applicant does not provide any support for the above arguments, thus the rejection is maintained.

Applicant states that the resistor-capacitor (R-C) combination 68, 70 of Fig. 12of Winebarger is not setup as an integrator". However, it would be clear to one of ordinary skill in the art that the above RC combination is in fact an integrator, and therefore does integrate the output of the comparator 58. To aide applicant's understanding that a resistor coupled to a high voltage, which is then coupled to a capacitor that is connected to ground is well-known in the art as an integrator, the examiner cites RC combination of R and C of Fig. 1 of Paschal et al. Clearly this RC circuit is connected the same way

as R4 and C2 of Winebarger. Additionally Paschal et al. discloses in Col. 2 lines 38-42 "At the output of the open collector NAND gate there is provided an **integrator circuit** comprised of a potential source, a resistor and capacitor is connected to a reference potential such as ground." The circuits RC circuits of Paschal et al. and Winebarger are the same, thus the RC circuit of Winebarger is an integrator. Therefore, it can clearly be seen that Winebarger's RC circuit of R4 and C2 is an integrator, and thus always integrates the output of 58.

Even if the signal input to the integrator is low, high, or an intermediate signal the RC circuit will integrate the output of 58. For example, if a 0 voltage value is input to the RC integrator of Winebarger, the integrator will still output an integrated value of 0, with respect to the amount of time the input value is 0 (integral of 0 is 0). Thus the shortfall signal is time integrated by R4 and C2. Additionally, it can be seen that the RC time delay is caused by the integrator circuit, thus while the integrator is time delaying the short fall signal (When POR is active high), the shortfall signal is being integrated (delayed) to provide a longer length POR signal. The recited language of claim 1 does not provide any limitation to the state of the shortfall signal (i.e. low or high), nor does it provide any limitation to the integration value of the output of the recited integrator. Thus, the rejection of claim 1 in view of Winebarger is withheld.

With respect to the rejection of claims 4-6 rejected under 35 USC 103(a) as being unpatentable over Winebarger, Examiner finds Applicant's arguments unpersuasive, as can be seen above the RC combination of R4 and C2 is an integrator, and the shortfall signal is time-integrated regardless of the output level of the

comparator 46. 46 can output an active low signal (V+ is under voltage), or an active high signal (V+ is above or at the required supply voltage), in which no matter the state input to the integrator R4 and C2 will output an integrated state. (i.e. integral of zero is zero). Additionally, applicant states that there is no point whatsoever in time-integrating this zero "shortfall signal", obviously it can be seen that the POR signal is longer due to the integrating (delaying) of the shortfall signal. Thus providing an adequately long POR signal. The recited language of claim 4 does not provide any limitation to the state of the shortfall signal (i.e. low or high), nor does it provide any limitation to the value of the output of the recited integrator. Thus, the obviousness rejection of claims 4-6 in view of Winebarger is withheld.

With respect to claims 1-2, and 4-7 rejected under 35 USC 103(a) as being unpatentable over Yoshimura (USPN 5,629,642) in view of Woods (USPN 6,259,285), Examiner finds Applicant's arguments unpersuasive. There is no recitation found in Yoshimura (USPN 5,629,642) that requires delay circuit 7 of Fig. 1 to be a "digital delay". In fact 7 is merely a generic delay circuit that encompasses all forms of delay. Also, it would be understood by one of ordinary skill in the art that "analog delay" circuits such as that of 130 of Fig. 1 of Woods do in fact create time-shifted delays. For instance, Applicant states that analog delay circuits effect "the rate at which the output voltage rises to a peak is delayed". Thus, if the peak voltage is delayed with time, then the logic high (signal equal to 1) would be delayed with time also, because the analog delay circuit would delay the amount of time required for a logic high to be achieved. Thus this would shift, with respect to time, when the input to 9 would achieve a logic

high, or conversely a logic low. Further, it would be understood that the delay times of 130 of Woods can be selected to the proper delay time by properly selecting the RC constants of 130 of Woods. Woods circuit is simply constructed, and used to rapidly filter erroneous signal levels, therefore one would be sufficiently motivated to use the specific error filtering delay circuit simply constructed delay circuit of Woods with Yoshimura generic delay circuit 7. Further it is notoriously well-known to combine RC delays with digital logic circuits. For instance, see Fig. 4 of Zhou et al., which discloses analog delay elements R with C input to NAND gate 403, thus combining an RC time delay with a digital circuit.

Allowable Subject Matter

Claims 9 and 10 are allowed

With respect to claim 9, there is no cited art that teaches the use of a control signal control switches of the discriminator circuit of Yoshimura. Also, there is no cited art that provides motivation for combining Yoshimura with a switched discriminator that accepts signals output form a comparator, and an integrated signal that is generated form a different output of a comparator. Thus claim 9 is allowed, and claim 10 is allowed based on the same reasoning as claim 3.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Terry D. Cunningham
Primary Examiner
Art Unit 2816

TH
April 17, 2006